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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ANDUJAR, LEONARDO	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,404	HSUAN, MIN-CHIH JOHN	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-30 and 49-60* is/are pending in the application.

4a) Of the above claim(s) *22-30* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *49-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of species 1 (fig.3a, claims 49-60) in the reply filed on 03/25/2005 is acknowledged. The traversal is on the ground(s) that the claim 49 is generic for species 1 and 2. This is not found persuasive because in the restriction requirement set forth in the Office Action sent on 01/29/2004, it was clearly established that the application contains patentably distinct species wherein each species is associated to each of the different embodiments depicted in the drawings. The examination of all the species is considered a serious burden since each species contains features that make them distinct and non-obvious over the other. Therefore, a complete and independent examination would be required for each of the disclosed species. Furthermore, the criterion for restriction of species is not whether the groups are coextensive but that the claims recite mutually exclusive characteristics of such species (MPEP § 806.04(f)). To traverse on the grounds that the species are not patentably distinct, the applicant should submit evidence, or identify such evidence in the record, showing the species to be obvious variants, or clearly admit on the record that this is the case. In either case, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) against the other invention(s). Because the applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Objections

2. Claim 49 is objected to because of the following informalities: the term unprocessed wafer is not adequate in view of the other claim limitations since the wafer is a processed wafer due to the fact that a hole has been formed. Appropriate correction is required.

3. Claim 52 is objected because "minimum size in the fabrication of active circuit" is an ambiguous terminology and is not based in any standard.

Claim Rejections

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Initially, and with respect to claim 49-52, note that a "product by process" claim is directed to the product per se, no matter how actually made. See In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which makes it

clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe, even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. In re Brown, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); In re Pilkington, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); Buono v. Yankee Maid Dress Corp., 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935). Note that Applicant has burden of proof in such cases as the above case law makes clear.

7. Claims 49, 50 and 52-59 are rejected under 35 U.S.C. 102(b) as being anticipated by, or in the alternative, under 35 U.S.C. 103(a) as obvious over Farnwoarth (US 5,973,396).

8. Regarding claim 49, Farnwoarth (e.g. fig. 1-2) shows a top surface and a bottom surface; and wherein the semiconductor wafer 10 is an unprocessed wafer having no active circuit layer or interconnect layers present top surface or the bottom surface of the semiconductor wafer, a plurality of vias 12/14 formed in the "unprocessed wafer", each having a via top portion being a the top surface of the unprocessed semiconductor wafer and extending through to a via bottom portion on the bottom surface of the unprocessed wafer; wherein a least some of the plurality of vias include an input/output interconnect structure 34 physically and electrically coupled to the via bottom portion, and the I/O interconnect structure is located within an area on the bottom surface of the

unprocessed wafer; and wherein the I/O interconnect is adapted such that an active circuit 22 can be electrically connected to another integrated circuit 22 (col.4/lls. 53-68 and col. 5/lls. 1-5). As to the grounds of rejection under section 103(a), the order of the method steps for making the semiconductor wafer including an integrated circuit scale package as recited in claim 49, are intermediate process steps that do not affect the structure of the final device. For example, it is not relevant if the device was fabricated starting with an unprocessed wafer or with a wafer having active circuit formed therein, or if the I/O interconnections are formed before the integrated circuit or after, as long as the final device includes all the structural limitations recited in the claim (i.e. vias, I/O interconnect structure, and an active circuit).

9. Regarding claim 50, Farnworth teaches that the vias are filled with a conductive material capable of withstanding a high temperature cycle associated with a manufacturing operation used to make the active circuit (i.e. silicon Au/Al doped; col. 4/32-34).

10. Regarding claims 52 and 53, Farnworth teaches most aspects discloses the claimed invention except for the size of the via such as 4 mils. It would have been an obvious matter of design choice to make the via disclosed by Farnworth having a size substantially larger than a minimum feature size used in the fabrication of integrated circuits 22 such as 4 mils diameter, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose, 105 USPQ 237 (CCPA 1955).*

11. Regarding claim 54, Farnworth teaches a passivation layer 50 formed on the top surface (e.g. fig. 1C).

12. Regarding claim 55, Farnworth teaches that the input/output interconnection structures include a plurality of solder bumps 36 and/pads 34.

13. Regarding claim 56, Farnworht teaches that the semiconductor includes a plurality of chip on scale packages (e.g. 110b/a).

14. Regarding claim 57, Farnworth teaches a plurality of integrated circuits 22 coupled to the plurality of chip scale packages (e.g. 110b/a).

15. Regarding claim 58, Farnworth shows a plurality of integrated circuit 22 on the semiconductor wafers are memory devices (col. 4/lls. 61-62).

16. Regarding claim 59, Farnworth shows a second I/O structure 24 on top of the semiconductor wafer (e.g. fig. 3).

17. Claims 51 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnwoarth (US 5,973,396) in view of Gnadinger (US 5,229,647).

18. Regarding claim 51, Farnworth teaches most aspects of the instant invention except for a vias filled with an insulating material capable of providing support for the semiconductor wafer during a manufacturing operation. Nevertheless, Gnadinger teaches a via 21 filled with an insulating material 24 (e.g. silicon oxide, silicon nitride) capable of providing support for the semiconductor wafer during a manufacturing operation. According to Gnadinger this type of embodiment is used to isolate the vias (col. 3/lls. 51-57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to fill the via disclosed by Farnworht with silicon

oxide/silicon nitride in accordance to Gnadinger's invention in order to avoid shout circuiting between adjacent vias.

19. Regarding claim 60, Farnworth teaches most aspects of the instant invention except for a via having a bottom portion substantially larger that a corresponding top portion. Nevertheless Gnadinger teaches a via 21 having a bottom portion substantially larger that a corresponding top portion (e.g. fig. 4). Additionally, this limitation, absent any criticality, is only considered to be an obvious modification of the shape of the via disclosed by Prior Art as the courts have held that a change in shape or configuration, without any criticality, is within the level of skill in the art as the particular shape claimed by applicant is nothing more than one of numerous shapes that a person having ordinary skill in the art will find obvious to provide using routine experimentation based on its suitability for the intended use of the invention. It would have been an obvious matter of design choice to make via disclosed by Farnworth having a bottom portion substantially larger that a corresponding top portion as suggested by Gnadinger since such a modification would have involved a mere change in the shape of a component. A change in shape is generally recognized as being within the level of ordinary skill in the art. See *In re Dailey, 149 USPQ 47 (CCPA 1976).*

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

21. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

22. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leonardo Andújar
Patent Examiner
Art Unit 2826
05/18/2005